



SRF Presentation, ISVLSI 2021, Tampa, Florida, USA, 7-9th July 2021



Machine Learning for VLSI CAD: A Case Study in On-Chip Power Grid Design

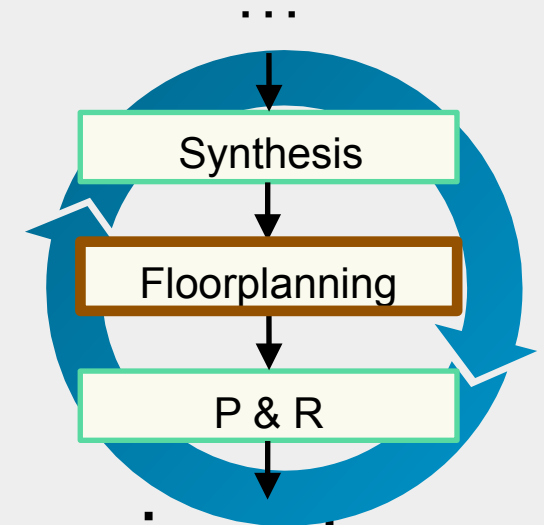
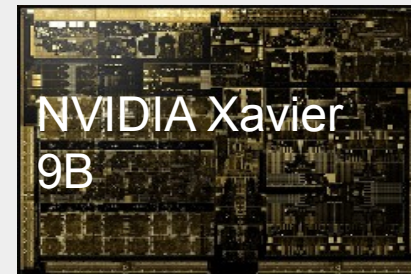
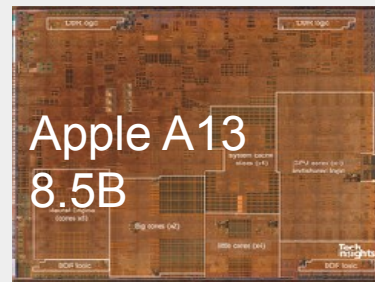
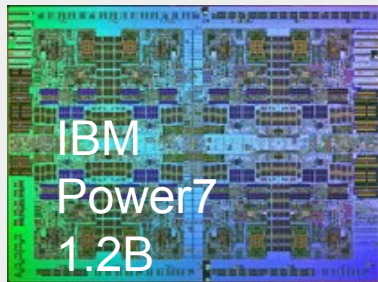
Sukanta Dey, IIT Guwahati

Overview

- Introduction
- Power Grid Design Challenges
- Contribution of my works
 - Probabilistic power grid analysis
 - Heuristic-based power grid design solutions
 - ML-based power grid design solutions
- Conclusion

Introduction

- Modern VLSI size and complexity keeps increasing.



- Power grid interconnects are designed in floorplanning stage.
- Power Planning plays a central role in the design flow.
 - Significant impact on design closure.
 - Check and satisfy IR drop and Electromigration margin.
 - Ensure reliability of chip/power grid.

Power Grid and Electrical Models

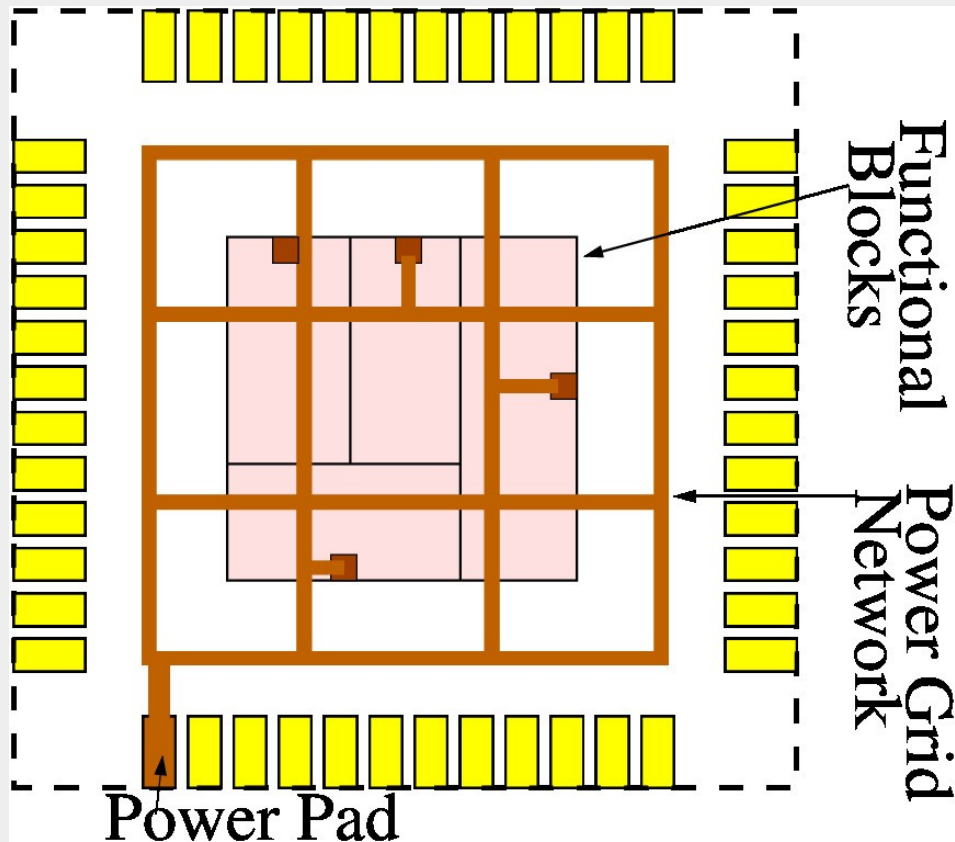


Fig: Toy model of SoC with Power Grid Connections

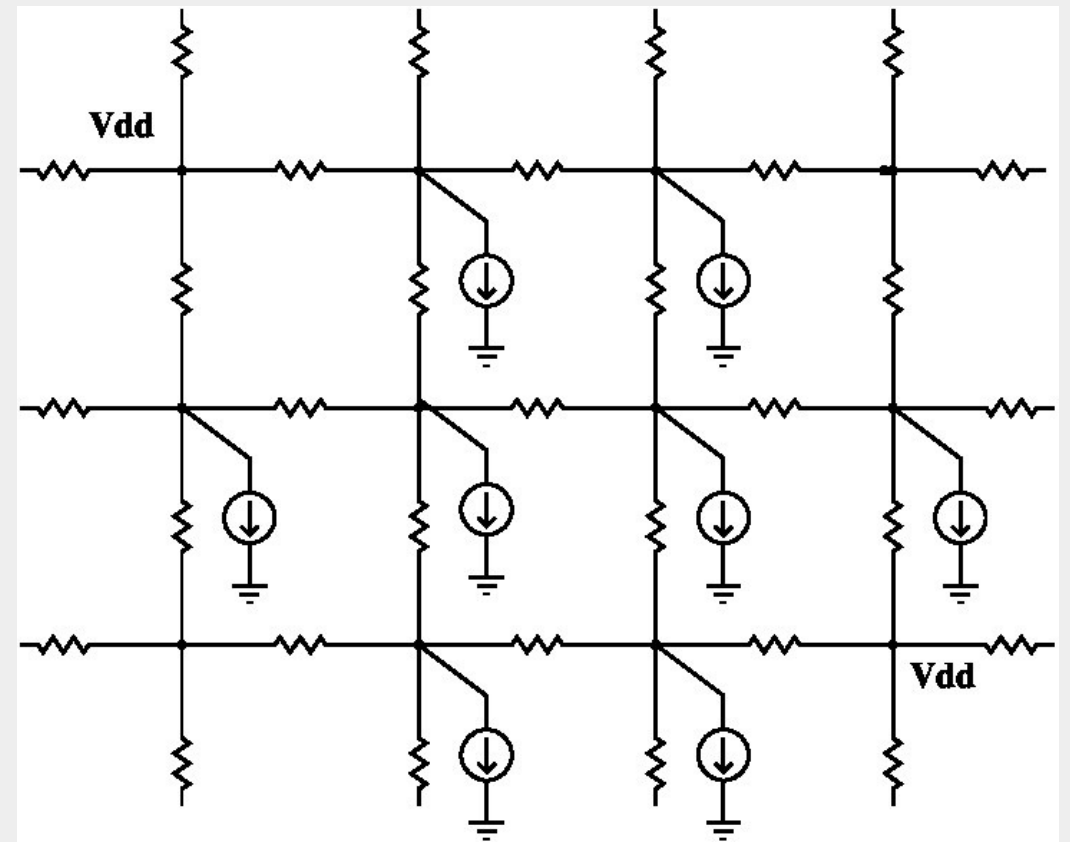


Fig: Steady-state electrical circuit model of power grids

Power Grid Design Challenges

- Large size of power grid circuit with increase in complexity.
- IR drop violations occur.
- Suffers from Electromigration violation.
- IR drop and Electromigration margin should be ensured.
- Optimal design point should be obtained.
- Existing methods are semi-automated or manual.
- Takes huge human labour and time for sign-off.
- There is a need to explore, for better design methodology/tool.
- AI/ML approach can be a good alternative.

Contributions of my work

- **Proposed work is divided in four parts:**
 - 1) Fast Probabilistic Power Grid Analysis Method.
 - 2) Design Space Exploration to find optimal design point using Metaheuristics
 - 3) ML-based Power Grid Design.
 - 4) ML-based Aging Prediction.

Fast Power Grid Analysis*

- Power grid network is converted into a unweighted graph.
- Objective is to speed up power grid analysis process.
- Our approach is based on random walk(RW)-based technique.
- We try to remove the self-loops of random walks.
- We adapted jumping strategy to speedup the convergence.
- Levy flight is used to incorporate the jumping strategy.
- To validate the method, it is tested with **49M** nodes of power grid network.
- We achieve max. speedup of **60X** over RW with $\leq 4\%$ error.

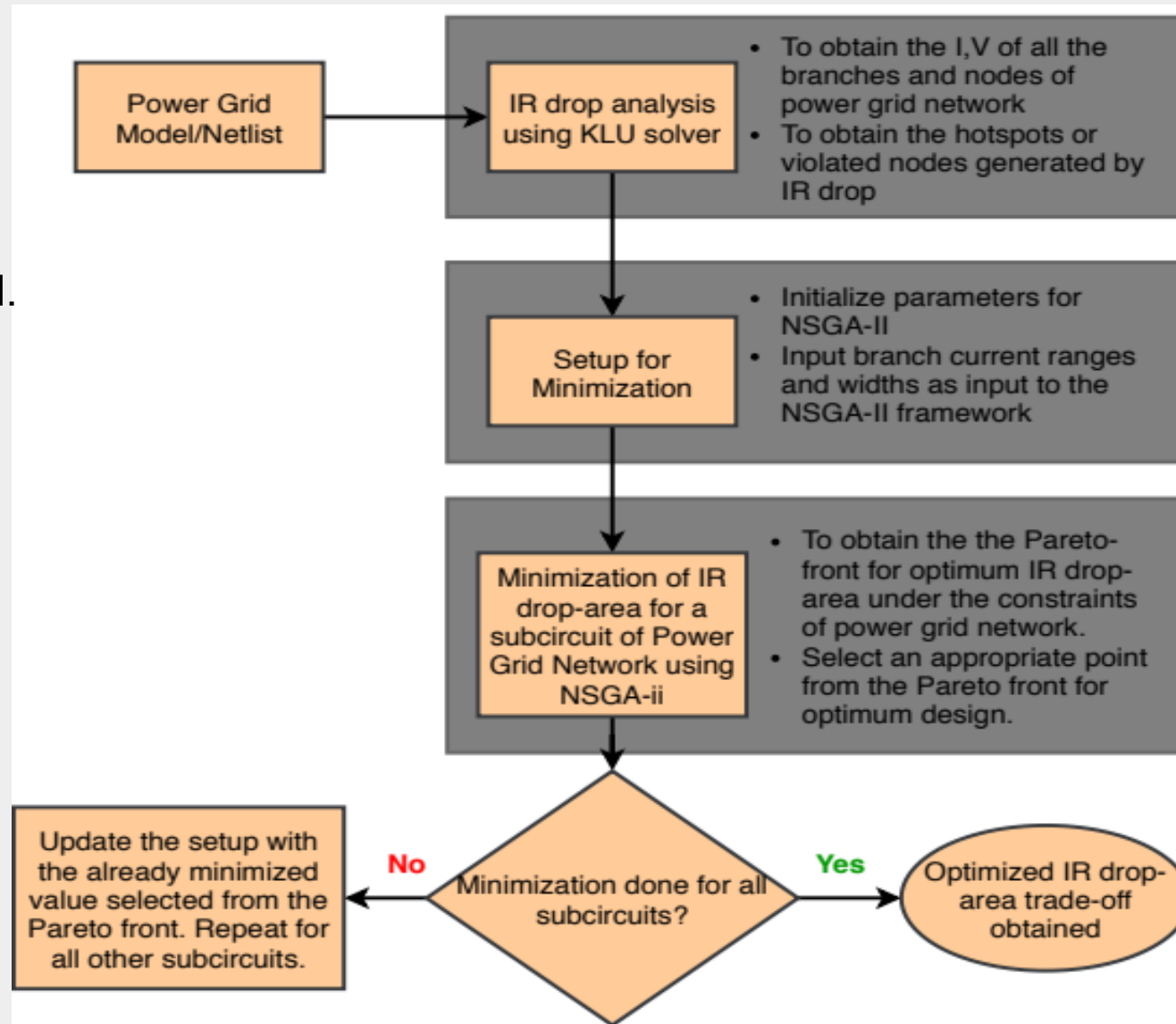
*Dey et al. "Markov Chain Model using Levy Flight for VLSI Power Grid Analysis", 30th International Conference on VLSI Design (VLSID 2017), Jan 2017.

Design Space Exploration

IR drop minimization increases metal routing area [Dey et al. IEEE ISVLSI 2018]

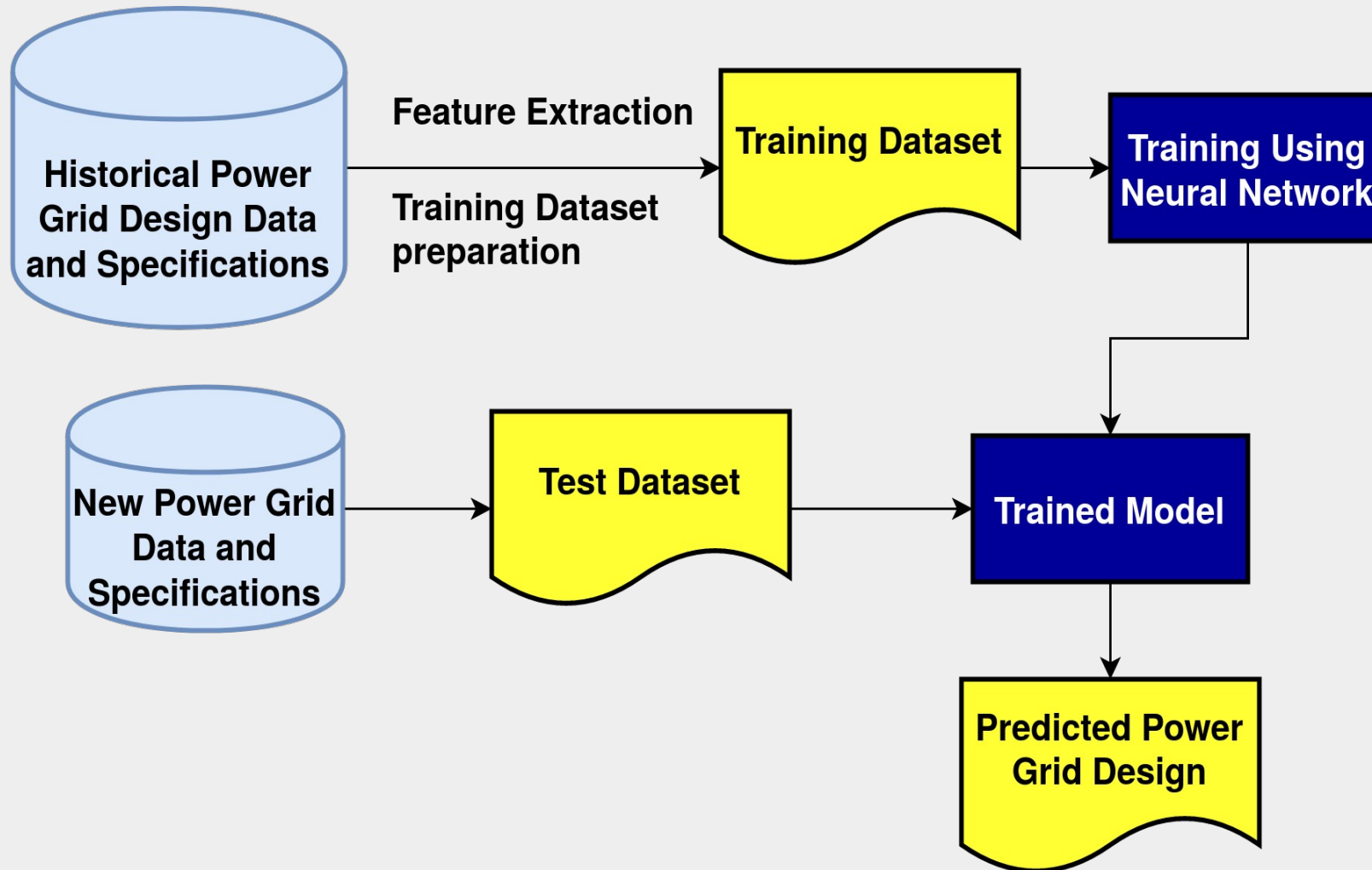
Two conflicting objectives:

IR drop and metal routing area



Optimum design point is obtained for a test case with **7.31% reduction** in worst-case IR drop and **8.51% reduction** in metal routing area [Dey et al. Elsevier MICPRO 2021]

ML-based Power Grid Design*



*Dey et al. "PowerPlanningDL: Reliability-Aware Framework for On-Chip Power Grid Design using Deep Learning" in DATE'20, April 2020.

Results

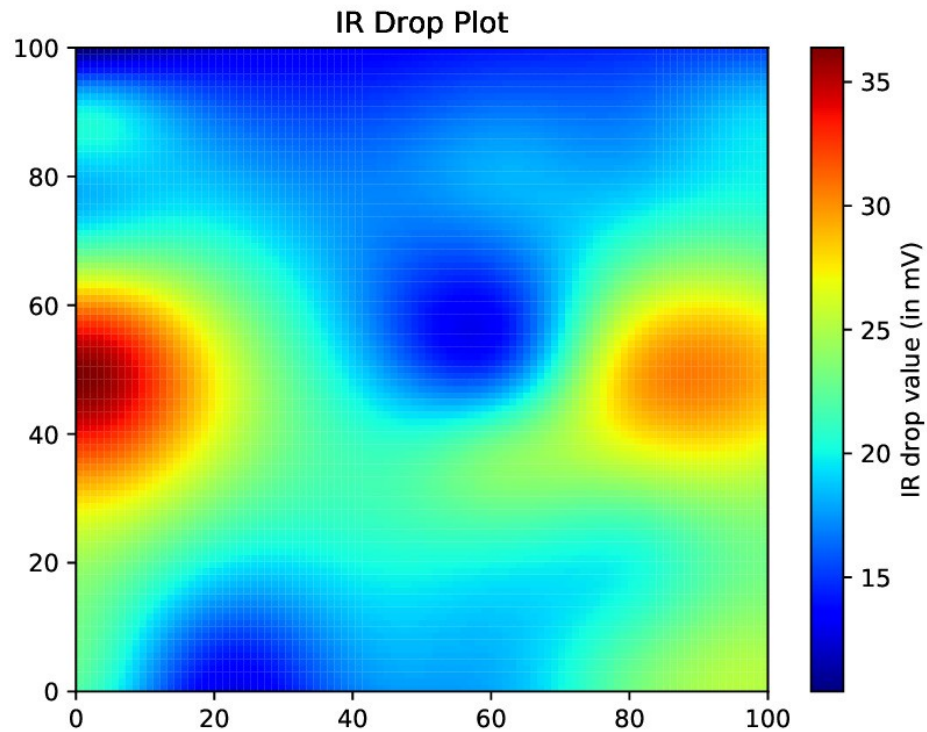


Fig: IR drop map of ibmpg2 using conventional method

Same quality of results using ML!

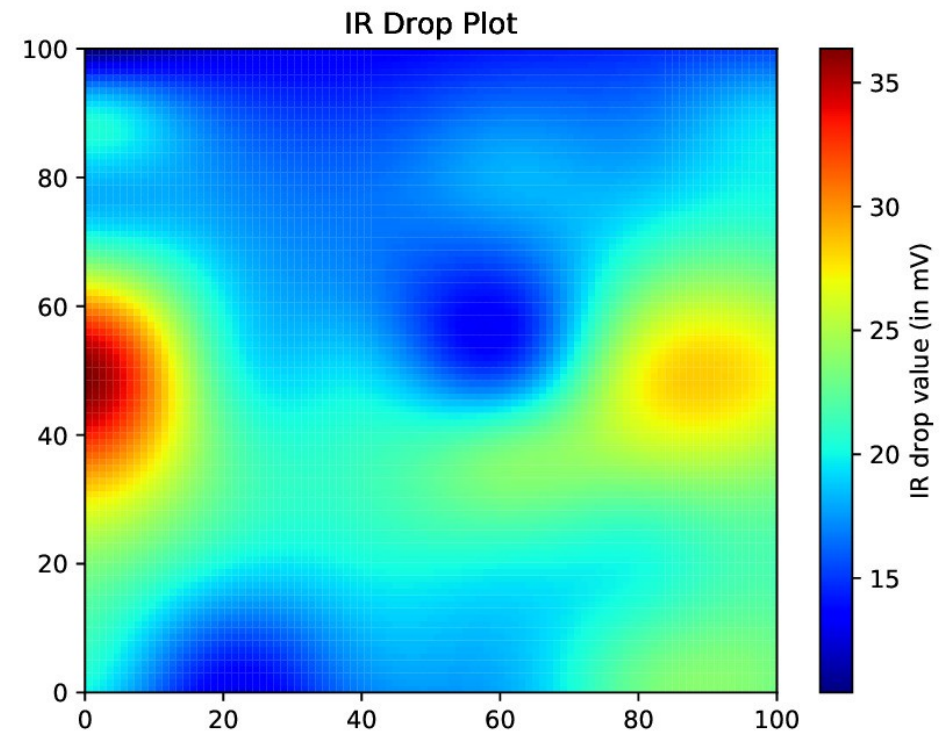
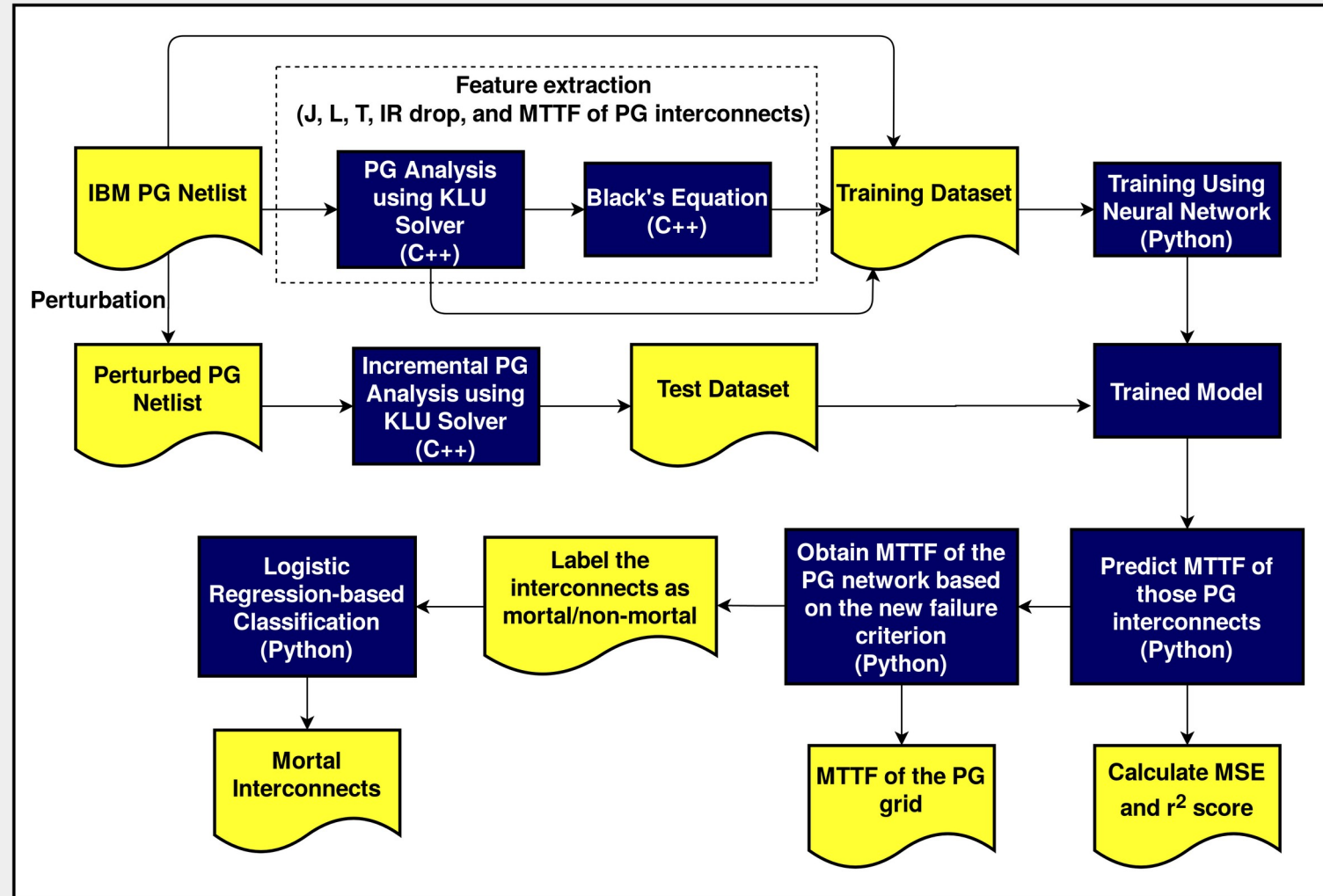


Fig: IR drop map of ibmpg2 using proposed ML approach

Error ~2%

Max speedup of ~5-6X

ML-based Aging-prediction*



*Dey et al. "Machine Learning Approach for Fast Electromigration Aware Aging Prediction in Incremental Design of Large Scale On-Chip Power Grid Network" in ACM TODAES, July 2020.

ML-based Aging-prediction

Methods	CPU Runtime (t) (Hours)					Speedup			
	TCAD2016 [19] (t_H)	ICCAD2017 [9] (t_{Ch})	TCAD2018 [10] (t_C)	IRPS2019 [30] (t_N)	Proposed (t_{ML})	$\frac{t_H}{t_{ML}}$	$\frac{t_{Ch}}{t_{ML}}$	$\frac{t_C}{t_{ML}}$	$\frac{t_N}{t_{ML}}$
PG Circuits									
<i>PG1</i>	0.02	0.02	0.001	0.000166	0.0001	200×	200×	10×	1.66×
<i>ibmpg1</i>	0.05	0.03	0.003	0.01000	0.0003	166.66×	100×	10×	33.33×
<i>ibmpg2</i>	0.11	0.31	0.04	0.02000	0.002	55×	155×	20×	10×
<i>ibmpg3</i>	5.83	4.27	0.41	0.07000	0.009	647.77×	610×	45.55×	7.77×
<i>ibmpg4</i>	14.71	6.81	2.31	0.11000	0.007	2,101.42×	972.85×	330×	15.71×
<i>ibmpg5</i>	0.69	0.25	0.06	0.03000	0.006	115×	41.66×	10×	5×
<i>ibmpg6</i>	1.75	2.07	0.79	0.23330	0.009	194.44×	230×	87.77×	25.92×
<i>ibmpgnew1</i>	16.78	0.42	1.24	0.08000	0.013	1,290.76×	32.06×	95.38×	6.15×
<i>ibmpgnew2</i>	15.32	2.60	0.43	0.06000	0.008	1,915×	325×	53.75×	7.50×
<i>PG2</i>	10.94	1.12	1.06	0.10166	0.010	1,094×	112×	106×	10.06×
<i>PG3</i>	-	-	-	0.13666	0.04200	-	-	-	3.25×
<i>PG4</i>	-	-	-	0.25666	0.10100	-	-	-	2.54×
Avg. Speedup						778×	277.85×	76.84×	10.74×

Our proposed ML-approach achieve speedup of 778X over [19], 278X over [9], 76.84X over [10], and 10X over [30].

ML-based Aging-prediction

Methods	MTTF (μ) (years)				
	TCAD2016 [19] (μ_H)	ICCAD2017 [9] (μ_{Ch})	TCAD2018 [10] (μ_C)	IRPS2019 [30] (μ_N)	Proposed (μ_{ML})
PG Circuits					
<i>PG1</i>	14.01	6.10	8.51	6.5	13.25
<i>ibmpg1</i>	12.55	6.50	10.91	7.0	12.10
<i>ibmpg2</i>	18.75	6.78	10.11	12.1	12.55
<i>ibmpg3</i>	31.96	6.66	9.95	6.7	12.25
<i>ibmpg4</i>	33.39	9.83	11.95	16.7	17.48
<i>ibmpg5</i>	25.16	6.54	6.63	6.3	10.33
<i>ibmpg6</i>	19.87	9.53	11.96	11.2	12.41
<i>ibmpgnew1</i>	25.96	13.24	11.64	13.2	14.56
<i>ibmpgnew2</i>	21.80	5.72	6.72	7.3	13.24
<i>PG2</i>	17.85	8.32	9.32	10.3	11.21
<i>PG3</i>	-	-	-	7.2	10.51
<i>PG4</i>	-	-	-	6.8	8.47

Accuracy wise our ML approach is the closest to accurate method of TCAD2016, and better than all other SOTA results.

Conclusion

- A fast and more effective power grid analysis technique is proposed, reducing the solving time of the circuit.
- We also attempt to design the power grid interconnects more efficiently by obtaining an optimum trade-off.
- This study includes machine learning techniques for power grid design and Electromigration-aware aging prediction of the power grid network.
- These works will help the power grid designer to obtain an initial idea of different design metrics and to handle the reliability issues in the process of designing cost-effective as well as reliable chip.

Thank you!