Machine Learning for VLSI CAD: A Case Study in On-Chip Power Grid Design

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***Abstract*—With the improvement of VLSI technology, on-chip power grid design is becoming more challenging than before. In this design phase of VLSI CAD, power grids are generated in order to make power and ground connections to transistors or logic blocks. However, due to the scaling of supply voltage and increase in the number of transistors per unit area of the chip, power grid design has become a considerable challenge. The two major issues encountered during power transfer via power grid are IR drop and Electromigration (EM). For a large chip, designers have to perform many iterations of a design in order to minimize IR drop and EM violations, which increases design cycle time. Recently, machine learning (ML) techniques have attracted the VLSI CAD community and are found to be very effective in solving VLSI CAD problems. However, very few works attempted to solve on-chip power grid design problem using machine learning. Therefore, this paper reviews some of the on-chip power grid design solutions using AI/ML approaches.**

***Index Terms*—IR Drop, Electromigration, Machine Learning, On-Chip Power Grid, VLSI CAD.**

I. Introduction

The design of high-performance chips in the semiconductor industry involves a vast human work-force, which also requires a substantial amount of time for realizing the design specifications. Following the market trends, the semiconductor industry advances with new efficient technology nodes in every alternate year. Therefore, it is imperative to reduce the design cycle time so that the chip design for the present technology node can be manufactured well before the subsequent technology node evolves into the market. Otherwise, the design may become obsolete once the new technology node appears in the market. Therefore, to reduce human efforts in the design cycle and to cope with the pace needed for chip designs, automating/semi-automating the design process is required. Artificial Intelligence (AI) and Machine Learning (ML) can play a massive role in the automation process of the chip design cycle. In this paper, we study different roles of AI and ML in some of the crucial aspects of the chip design. To be specific, we have discussed how different learning techniques can be implemented to improve chip design tasks, especially how AI and ML can be adapted to improve the design of on-chip power grid interconnects. On-Chip power grid interconnects are the metallic interconnects within a chip that is used to deliver power supply voltage from the power supply pads to the underlying transistors. The major challenges faced during power transfer are the following two:

IR drop: It denotes voltage drop that occurs across metallic interconnects when current is passed through it. If the IR drop exceeds a certain threshold, the underlying transistors do not get the adequate voltage that is intended by it.

Electromigration: It is the movement of metal atoms due to the exchange of momentum from the electrons to the metal atoms. A higher current density causes it. Due to the electromigration voids and hillocks are formed in the metal lines, which can short circuit or open circuit some of the metal interconnects causing malfunctioning of the chip.

Motivations: If these above two challenges are not handled during the design time, the chip may malfunction, or the chip's longevity is reduced. This phenomenon decreases the reliability of the chip. The primary design challenge in the design of the power grid interconnects is that it takes a huge amount of circuit analysis time for a large-scale power grid network. Further, iteratively it needs to perform circuit analysis in order to optimally find the widths of the power grid interconnects. This increases the design cycle time. Also, it consumes a significant working hour. Existing methods of designing power grid are time-consuming as it checks for IR drop and EM violations over many iterations of the design cycle. Moreover, recent Intelligent Design of Electronic Assets (IDEA) program sponsored by DARPA in 2018 [1], focuses on creating a "no human in the loop", 24-hour turnaround layout generator for System-On-Chips. Therefore, in this paper, we have demonstrated various AI and ML techniques to improve the power grid interconnects' design cycle. The contributions[1] of the paper are mainly divided in four parts described each in subsequent sections. Before describing the contributions, it is necessary to know the preliminaries of AI/ML approaches.

II. Preliminaries

A. On-Chip Power Grid Design and Related Works

VLSI Physical Design is an integral part of VLSI CAD, where the layouts are generated from its circuit specifications. Initially, estimated designs of power grid lines are created in the floorplan stage, even before the placement of logic blocks. Subsequently, power grid modeling is done in order to analyze the power grid designs. During the modeling stage, power grid lines are converted into equivalent electrical models. In this paper, we have used only resistive models of power grid. The logic blocks are modeled as current sources connected to ground. Once the modeling is done, circuit analysis is performed to observe the voltage and currents in the power grid, which is known as power grid analysis. Using the voltage

[1]This paper is based on author S. Dey's dissertation, a more detailed text can be found in [2].

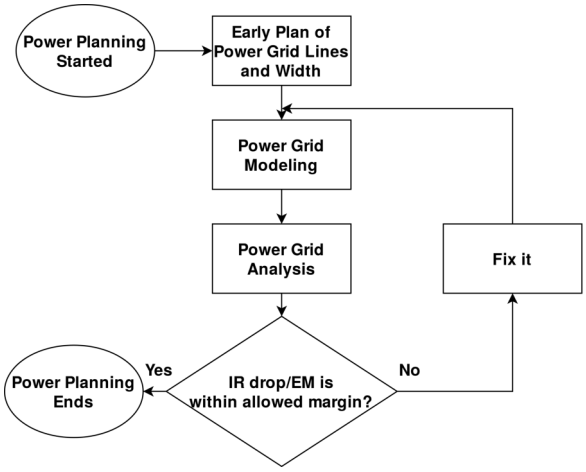


Fig. 1. On-Chip Power Grid Design Flow

and current obtained from the power grid analysis stage, IR drop and Electromigration (EM) violations are checked. If it is within acceptable margin power planning stage is completed, or else power grid designs need to be fixed. Achieving a reasonable margin of IR drop and EM violations for a large power grid is a challenge, which requires many iterations of the design cycle. In order to make the power planning cycle faster, in this paper, we propose some solutions using AI/ML approaches. Also, there are many efforts in the VLSI CAD community to adapt Machine Learning techniques [3], [4]. However, only a few works attempted the on-chip power grid design problem using the machine learning technique. Therefore, discussion of this paper is more about our contributions in power grid design using AI/ML approaches.

A toy model of power grid network and equivalent resistive circuit model are shown in Fig. 2. It is to be noted that by "power grid", we mean power and ground grid as a whole. However, in general, power and ground grids are both separate network; connected to V_{DD} and V_{SS} (or ground) sources, respectively.

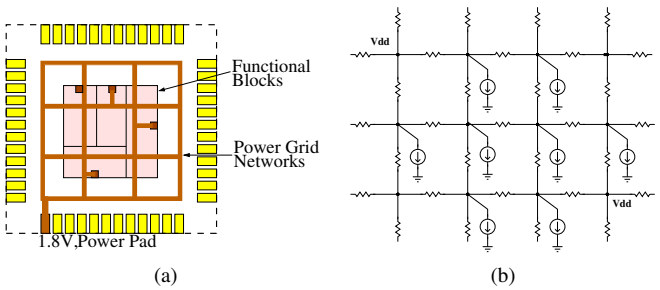


Fig. 2. (a) A representational view of on-chip power grid network connected with the functional blocks. These functional blocks are consist of transistors-based circuits. (b) Resistive network model of PGN. circuit

B. AI/ML Techniques

Artificial Intelligence (AI) and Machine Learning (ML) have gained significant attention in the last decade due to the substantial breakthrough in the deep learning models in predicting complex tasks. Another primary reason behind the success of the deep learning model is the advent of the many-core architectures (GPU), which helped the training of models in feasible time in order to predict complex tasks. However, when we talk about AI/ML, it not only means the deep learning. AI means any system that possesses intelligent decision-making capability. Further, those decision-making systems, where learning happens from its previous or historical data/experience, are known as machine learning systems. Generally, the class of AI can be broadly divided into three categories based on their type of learning. These are:

- Probabilistic Learning
- Metaheuristic Learning
- Machine Learning

1) Probabilistic Learning: In probabilistic learning, the entities perform the tasks depending on the estimated probabilities of the events. The objective is to create stochastic models that describe a series of feasible occasions. In order to do so, transition probabilities for different sets of possible events are evaluated. There are several probability models in the literature, such as Markov chain models, Queuing models, Petri nets. In Section III, we use stochastic approach to analyze the power grid analysis problem. The power grid network is modeled as a graph and mapped as a Markov chain model. For faster traversal of the power grid network, we use Lévy flight. Our proposed approach helps in obtaining faster convergence in power grid analysis.

2) Metaheuristic Learning: In metaheuristic learning, the objective is to create mathematical cost functions. Subsequently, obtain the cost function's optimized value and its corresponding decision variables by employing heuristic search techniques. For generating the search space, many random points are generated. The cost function is evaluated in all those points of the search space. Subsequently, various search techniques are employed for efficient search. These search strategies are problem-specific. For different kinds of problems, different search strategies become suitable. There is not a single generalized search technique that can give the best result for all problems. Moreover, these search strategies can find a near-optimum solution for any complex multimodal problems. In Section IV, we have employed metaheuristic learning in order to obtain the optimum design space exploration of the power grid design. For that, we use cooperative coevolution, and nondominated sorting genetic algorithm (NSGA-II) approaches.

3) Machine Learning: Machine Learning mostly includes learning from data. Here the underlying philosophy is to create an inference model from the dataset. Subsequently, one is required to predict samples for a new set of specifications. Machine Learning is majorly divided into two major classes:

- Supervised Learning.
- Unsupervised Learning.

In supervised learning, all the training samples of the dataset are labeled. In unsupervised learning, the dataset is unlabelled. There are different traditional machine learning models, such as SVM, Random Forest, Gaussian Process, Artificial Neural Network. These models generally don't perform well for complex prediction tasks. Subsequently, researchers in 2010s have developed and achieved massive success with the deep

neural network (DNN) having multiple hidden layers. DNN can perform prediction tasks on imagenet dataset with near-human level accuracy, which gives rise to the field of deep learning. Both supervised and unsupervised, several emerging deep learning models are coming up as the time progresses. The work of this paper is limited only to the supervised learning models. In supervised learning, a model is created depending on these labeled samples in order to predict the labels of new test samples. Another essential part of the machine learning model is the feature set. We have generated a dataset with proper feature selection using IBM power grid benchmarks for our work in this paper [5]. We employ this dataset in order to create deep neural network-based machine learning models, which are described in Section V and Section VI.

Proposed approaches of the paper are mentioned in next four subsequent sections. At first, Section III describes a fast probabilistic approach of on-chip power grid analysis. Section IV describes a metaheuristic approach using NSGA-II to obtain an optimum trade-off between IR drop and metal routing area for on-chip power grid design. Subsequently, in Section V, the first proposal of ML approach is demonstrated for on-chip power grid design. Finally, in Section VI, again, the first proposal of ML is presented to predict EM-aware lifetime of on-chip grid network. For experimental purposes, IBM power grid benchmarks [5] are employed. The experiments are performed using C/C++ and Python languages along with machine learning libraries scikit-learn and Tensorflow.

III. Power Grid Analysis using Probabilistic Approach:

Generally, power grid network is modeled as the RLC circuit to detect the hotspots. We have considered only the resistive model as we are only interested in a steady-state analysis. Hotspots are the affected areas of the power grid network where the voltages level goes below a specific threshold value. Hotspots are generated due to the voltage drop across the metal lines known as IR drop. Hotspots are identified as those nodes whose voltage values drop below a specific threshold value. Therefore basic circuit analysis methods are used in the literature to detect the hotspots. However, with the increase in the size of the circuit, the traditional methods of the literature are not able to perform circuit analysis in an effective way, resulting in huge time and memory resource consumption. Therefore, researchers have used heuristic-based methods such as Random walk [6] to perform circuit analysis, which has become very famous among the research community. To make circuit analysis more faster and effective, we use a method based on Lévy Random Walk [7] here to detect the hotspots created by the voltage drop. Circuit analysis consists of steady-state analysis and transient analysis. In this paper, we have only considered steady-state analysis. In the steady-state analysis, only the resistive elements of the circuits are considered. From the resistive electric networks, linear system of equations are formed $GV = I$ where G, V, and I are the conductance matrices, voltage vectors, and current vectors respectively, which is then solved using traditional solvers such as Gaussian Elimination, Gauss-Jordan etc. Random walk-based heuristic method is also used to solve the linear equations system in an analogous way, which has shown better performance in circuit analysis with respect to time than the traditional solvers within the acceptable limit of error. However, one demerit is that Random Walk depends on the random probability values to converge (or to find the Vdd homes). Therefore, it keeps traversing into some closed loop of nodes without finding the destination home, which unnecessarily increases the power grid network's solving time. To make the circuit analysis more faster, Levy Random Walk method is employed which uses jumping strategy from one node to the other to make the traversal of the whole power grid network faster and reduces time significantly. Our proposed solution also removes the problem of trapping in a loop of nodes. To compensate for any error due to the introduction of Levy Random walk, effective resistance between two points of the power grid is calculated using the formula given in [8] and embedded in the equations of random walk. Finally, the performance of the proposed scheme is validated on standard power grid benchmarks, which show significant speedup. Our experimental results on large-scale power grid benchmarks show speedup over state-of-art solutions as shown in Table I, with a maximum error of ($\leq$4%). More details of the work of this section can be found in [9].

TABLE I
Speedup Analysis of using Lévy flight Approach on CPU

Nodes	t_{RW} (s)	t_{GS} (s)	t_{HLS} (s)	t_{levy} (s)	Speedup (t_{RW}/t_{levy})	Speedup (t_{GS}/t_{levy})	Speedup (t_{HLS}/t_{levy})
pgckt_10K	0.06	0.07	0.22	0.04	1.50×	1.75×	5.50×
pgckt_40K	0.30	0.36	0.82	0.17	1.76×	2.11×	4.82×
pgckt_90K	0.65	1.62	1.84	0.30	2.16×	5.40×	6.13×
pgckt_250K	1.92	6.78	6.06	0.86	2.23×	7.88×	7.04×
pgckt_640K	7.98	19.31	20.00	2.19	3.64×	8.81×	9.13×
pgckt_1M	18.95	27.85	39.55	3.51	5.39×	7.93×	11.26×
pgckt_4M	297.21	117.76	154.78	14.61	20.34×	8.06×	10.59×
pgckt_9M	1513.4	272.74	349.66	33.88	44.66×	8.05×	10.32×
pgckt_16M	3326.44	486.03	651.15	61.49	54.09×	7.90×	10.58×
pgckt_25M	6263.80	760.10	1034.36	112.85	55.50×	6.73×	9.16×
pgckt_36M	9800.35	1094.01	1562.71	167.63	58.46×	6.52×	9.32×
pgckt_49M	14065.90	1498.20	2430.38	232.91	60.39×	6.43×	10.43×

IV. Design Space Exploration of Power Grid using Heuristic Approach:

This section deals with design space exploration (DSE) of on-chip power grid for obtaining optimum design point. The design space exploration of different critical power grid design objectives is achieved by using metaheuristic. The primary objective is to reduce IR drop hotspot. In our preliminary work [10], we have observed that we can achieve IR drop minimization by increasing the metal routing area. Subsequently, we also observe that if metal routing area minimization increases IR drop [11]. Therefore, we form a multiobjective optimization problem with IR drop and metal routing area as two primary objectives. We solve this using nondominated sorting genetic algorithm II (NSGA-II) metaheuristic. The proposed approach is described in Fig. 3. The power grid network is divided into many subcircuits, and optimization is done in each subcircuits to find Pareto optimal solutions for each subcircuits. When the optimization is done for all subcircuits, we consider that the optimum design point is obtained. From the IR drop map shown in Fig. 4, we can recognize the red hotspots have been reduced using the proposed DSE framework. With our proposed DSE framework, we can observe that we have achieved a tradeoff between IR drop and metal routing area as shown in Table II. More details about this work can be found in [12] [10] [11].

TABLE II
COMPARATIVE STUDY OF PROPOSED DSE FRAMEWORK WITH WORK OF SINGLE-OBJECTIVE FORMULATION

PG_circuits	Before optimization	single-objective formulation			Proposed DSE		
	$V_{\text{IR worst initial}}$ (V)	$V_{\text{IR worst}}$ (V)	$\Delta V_{\text{IR worst}}$	ΔA	$V_{\text{IR worst}}$ (V)	$\Delta V_{\text{IR worst}}$	ΔA
$ibmpg2$	0.0369	0.0263	-28.72%	+17.87%	0.0342	-7.31%	-8.51%
$ibmpg3$	0.2438	0.1879	-22.92%	+14.33%	0.2230	-8.53%	-8.20%
$ibmpg4$	0.0086	0.0041	-52.32%	+22.65%	0.0075	-12.79%	-7.92%
$ibmpg5$	0.0690	0.0431	-37.53%	+18.27%	0.0610	-11.59%	-7.59%
$ibmpg6$	0.2063	0.1529	-25.88%	+15.82%	0.1881	-8.82%	-7.32%

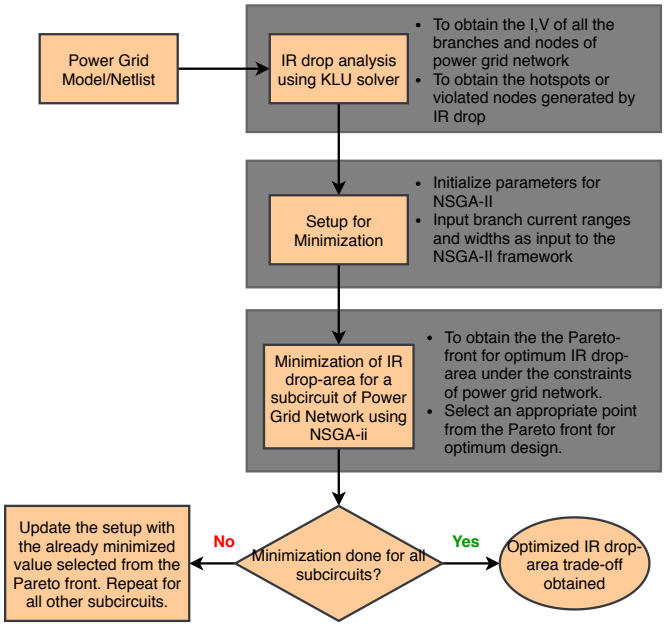
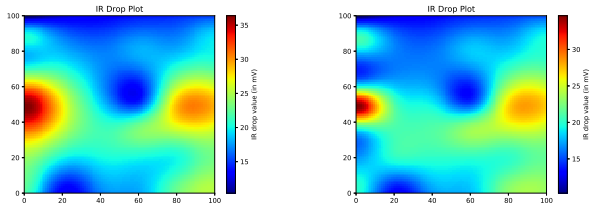


Fig. 3. Proposed Design Space Exploration Framework Flow



(a) (b)

Fig. 4. IR drop profile of $ibmpg2$ circuit (a) before optimization, (b) after optimization

V. POWER GRID DESIGN USING MACHINE LEARNING:

This proposal describes how the machine learning approach can be incorporated for designing a reliable on-chip power grid. We propose the first-ever machine learning model for on-chip power grid design. The flow of the proposed approach is shown in Fig. 5. We generated datasets using IBM power grid benchmarks [5]. The feature selection is made by evaluating the r^2 score of various sets of input and output features. Finally, for our machine learning model, we consider I_d current source at (x,y) point and its coordinates (x,y) as input feature for a metal line and width of metal lines as output feature.

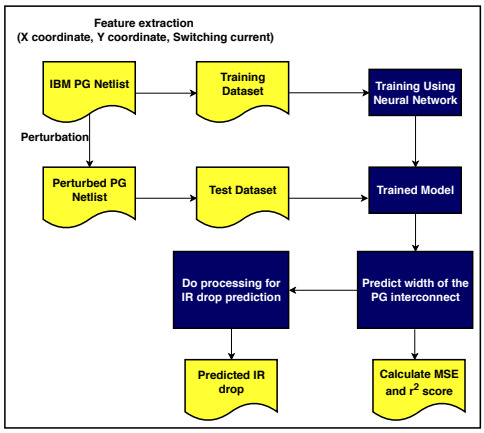


Fig. 5. ML-based Power Grid Design Flow

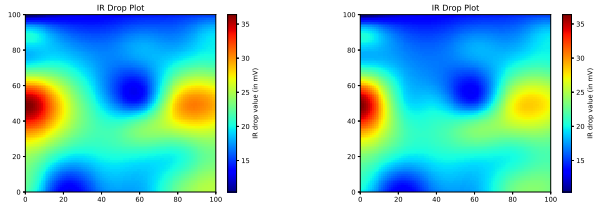
Considering these feature sets, we constructed datasets. We employ a neural network-based supervised machine learning technique to predict the optimum widths of the metal lines of the power grid network. The neural network is trained using the generated dataset, and a perturbed version of dataset is used as testset for testing the ML approach. Once the optimum widths are obtained with the help of ML approach, we obtain the IR drop map using Kirchoff's rule. We achieve a similar IR drop map with ML approach as compared to IR drop map obtained from the conventional approach as shown in Fig. 6. The worst-case IR drop for all other $ibmpg$ benchmarks are listed in Table IV, which shows that ML approach produces very close results to the conventional approach. We have also achieved a maximum speedup of ∼5-6× over the conventional approach as shown in Table III. More details about this work can be found in [13].

TABLE III
COMPARATIVE STUDY OF CONVERGENCE TIME FOR CONVENTIONAL POWER PLANNING APPROACH AND PROPOSED ML FRAMEWORK

	Time (sec)		Speedup
PG circuits	Conventional	PowerPlanningDL	$\frac{\text{Time}_{\text{Conventional}}}{\text{Time}_{\text{PowerPlanningDL}}}$
$ibmpg1$	6.85	3.56	1.92×
$ibmpg2$	23.46	11.88	1.97×
$ibmpg3$	29.50	8.07	3.59×
$ibmpg4$	52.4	11.83	4.42×
$ibmpg5$	74.80	12.74	5.87×
$ibmpg6$	97.5	17.41	5.60×
$ibmpgnew1$	102.58	21.50	4.77×
$ibmpgnew2$	48.60	10.86	4.47×

TABLE IV
COMPARATIVE STUDY OF WORST-CASE IR DROP USING CONVENTIONAL POWER PLANNING APPROACH AND PROPOSED ML FRAMEWORK

	Worst-case IR drop (mV)	
PG circuits	**Conventional**	**PowerPlanningDL**
$ibmpg1$	69.8	68.2
$ibmpg2$	36.3	36.1
$ibmpg3$	18.1	18.0
$ibmpg4$	4.0	4.1
$ibmpg5$	4.3	4.2
$ibmpg6$	13.1	13.0



(a) (b)

Fig. 6. IR drop map of $ibmpg2$ circuit (a) Conventional method (b) Proposed ML method

VI. AGING PREDICTION OF POWER GRID DESIGN USING MACHINE LEARNING:

In this section, our proposed work depicts a machine learning approach for computing lifetime of the power grid network in its design phase. With the improvement in VLSI technology, Electromigration(EM) sign-off has grown to be a big challenge, necessitating a substantial amount of time for an incremental change in the power grid (PG) network design in a chip. In this work, for the first time, we present a machine learning approach to obtain the EM-aware aging prediction of on-chip PG network. We employ neural network-based regression as our core machine learning technique to immediately predict a perturbed PG network's lifetime. Here, also we propose a supervised learning model as shown in Fig. 7. Similar to Section V, the feature selection is made by evaluating $r^2 score$, and dataset is created using IBM power grid benchmarks. For the test dataset, we have made some perturbations in the dataset in order to bring new samples to the test dataset. We also introduce a new failure criterion that produces a better MTTF value. Possible EM-affected metal segments of the PG network are detected by using a logistic-regression-based classification machine learning technique. We achieve notable speedup over the state-of-the-art results as shown in Table VI. Our predicted MTTF values are also close to the accurate method of [14] as shown in Table V. More details about this work can be found in [15].

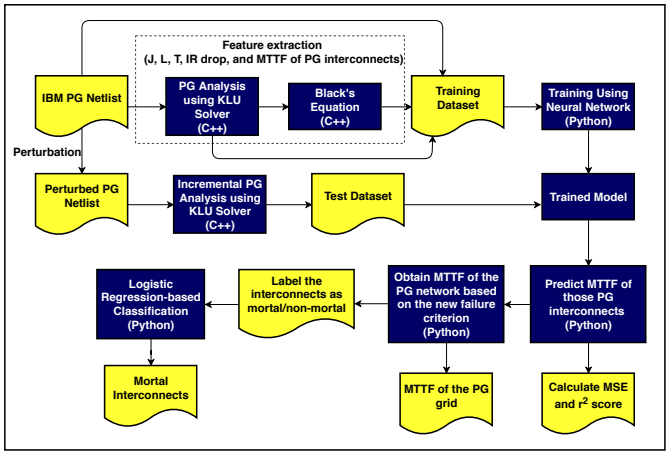


Fig. 7. ML-based Electromigration-aware aging prediction flow

TABLE V
COMPARATIVE STUDY OF MTTF FOR OUR PROPOSED ML-BASED APPROACH WITH WORKS OF [14], [16]–[18] FOR IBM POWER GRID BENCHMARKS.

	MTTF (μ) **(years)**				
Methods	**TCAD2016 [14]** (μ_H)	**ICCAD2017 [16]** (μ_{Ch})	**TCAD2018** [17] (μ_C)	**IRPS2019** [18] (μ_N)	**Proposed** (μ_{ML})
PG Circuits					
$PG1$	14.01	6.10	8.51	6.5	13.25
$ibmpg1$	12.55	6.50	10.91	7.0	12.10
$ibmpg2$	18.75	6.78	10.11	12.1	12.55
$ibmpg3$	31.96	6.66	9.95	6.7	12.25
$ibmpg4$	33.39	9.83	11.95	16.7	17.48
$ibmpg5$	25.16	6.54	6.63	6.3	10.33
$ibmpg6$	19.87	9.53	11.96	11.2	12.41
$ibmpgnew1$	25.96	13.24	11.64	13.2	14.56
$ibmpgnew2$	21.80	5.72	6.72	7.3	13.24
$PG2$	17.85	8.32	9.32	10.3	11.21
$PG3$	-	-	-	7.2	10.51
$PG4$	-	-	-	6.8	8.47

Overall in this paper work, it is demonstrated that AI/ML approaches can be a good alternative for the traditional power grid design approaches, which is fast and can speedup the overall design cycle for future intricate SoC design.

VII. SCOPE FOR IMPROVEMENT

The work proposed in Section III is applicable to regular large power grids. In order to adapt the proposed approach of Section III for practical cases of power grid circuits, it is necessary to have an analytical equivalent resistance model for practical non-uniform power grids.

The methods presented in Section IV and Section V are designed with the assumption that it is a two-layer power grid. However, the work can be extended for a multi-layer power grid with proper formulation and calibration.

As mentioned before, the machine learning approaches are found to produce good results for incremental designs. Therefore, further work is required in order to design fully automated machine learning solutions for on-chip power grid design.

VIII. CONCLUSION AND FUTURE WORKS

The work of this paper is motivated towards improving the on-chip power grid design methodology with Artificial Intelligence and Machine Learning techniques as viable options. Towards this, we work on major two design challenges of the on-chip power grid design phase. These two challenges are IR drop and Electromigration issues. Both of these issues increase failure probability of the power grid network as well as the chip. Existing works mostly solve the IR drop analysis with linear algebraic methods which is a time-consuming process for the large power grid networks. Also, it is necessary to optimize the power grid design considering various critical design objectives. Existing works of literature do not address these multiobjective optimization issues, instead, the work of

TABLE VI
COMPARATIVE STUDY OF CPU RUNTIME FOR OUR PROPOSED ML-BASED APPROACH WITH WORKS OF [14], [16]–[18] FOR IBM POWER GRID BENCHMARKS.

	CPU Runtime (t) (Hours)					**Speedup**			
Methods	**TCAD2016** [14] (t_H)	**ICCAD2017** [16] (t_{Ch})	**TCAD2018** [17] (t_C)	**IRPS2019** [18] (t_N)	**Proposed** (t_{ML})	$\frac{t_H}{t_{ML}}$	$\frac{t_{Ch}}{t_{ML}}$	$\frac{t_C}{t_{ML}}$	$\frac{t_N}{t_{ML}}$
PG Circuits									
$PG1$	0.02	0.02	0.001	0.000166	0.0001	200×	200×	10×	1.66×
$ibmpg1$	0.05	0.03	0.003	0.01000	0.0003	166.66×	100×	10×	33.33×
$ibmpg2$	0.11	0.31	0.04	0.02000	0.002	55×	155×	20×	10×
$ibmpg3$	5.83	4.27	0.41	0.07000	0.009	647.77×	610×	45.55×	7.77×
$ibmpg4$	14.71	6.81	2.31	0.11000	0.007	2101.42×	972.85×	330×	15.71×
$ibmpg5$	0.69	0.25	0.06	0.03000	0.006	115×	41.66×	10×	5×
$ibmpg6$	1.75	2.07	0.79	0.23330	0.009	194.44×	230×	87.77×	25.92×
$ibmpgnew1$	16.78	0.42	1.24	0.08000	0.013	1290.76×	32.06×	95.38×	6.15×
$ibmpgnew2$	15.32	2.60	0.43	0.06000	0.008	1915×	325×	53.75×	7.50×
$PG2$	10.94	1.12	1.06	0.10166	0.010	1094×	112×	106×	10.06×
$PG3$	-	-	-	0.13666	0.04200	-	-	-	3.25×
$PG4$	-	-	-	0.25666	0.10100	-	-	-	2.54×
Avg. Speedup						778×	277.85×	76.84×	10.74×

literature only considers area minimization as the power grid optimization solution. The use of simple linear programming techniques for optimizing the power grid is also not a good option for large power grid networks. Further, it is necessary to obtain the electromigration-aware aging prediction of the power grid networks, during the design phase itself. Existing physics-based approaches take a large amount of time for design sign-off. Therefore, for all the problems of power grid design, a fast solution is required. We have discovered that the AI/ML techniques help in fast sign-off of the power grid design problems.

The contributions of this paper can be extended in several ways. Some of the possible future research directions are listed below:

- The machine learning-based proposed works in this paper uses manual feature engineering. In future, automatic feature engineering can be employed to further automating the learning process of the power grid design.
- This paper profoundly concentrated on formulating the problems as supervised learning problems. In the future, power grid design problems can be formulated as unsupervised learning problems and solved using the emerging learning approaches such as Variational Autoencoder, Generative Adversarial Network etc.
- Other objectives of the power grid design can further be solved using AI/ML approaches.
- Parallelization techniques can be explored for fast sign-off of the power grid analysis.
- Thermal Issues of PG Design can be explored.
- Extension of the works to PG Design of 3D IC.
- This paper's proposed methods can also be extended to electrical grid design (used for delivering electricity from producers to consumers), with appropriate changes.

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