Design Methodology for On-Chip Power Grid Interconnect: AI/ML Perspective

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by

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Conclusions and Future Works

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7.1 Introduction

The work of this thesis is motivated towards improving the on-chip power grid design methodology with Artificial Intelligence and Machine Learning techniques as viable options. Towards this, we work on major two design challenges of the on-chip power grid design phase. These two challenges are IR drop and Electromigration issues. Both of these issues increase failure probability of the power grid network as well as the chip. Existing works mostly solve the IR drop analysis with linear algebraic methods which is a time-consuming process for the large power grid networks. Also, it is necessary to optimize the power grid design considering various critical design objectives. Existing works of literature do not address these multiobjective optimization issues, instead, the work of literature only considers area minimization as the power grid optimization solution. The use of simple linear programming techniques for optimizing the power grid is also not a good option for large power grid networks. Further, it is necessary to obtain the electromigration-aware aging prediction of the power grid networks, during the design phase itself. Existing physics-based approaches take a large amount of time for design sign-off. Therefore, for all the problems of power grid design, a fast solution is required. We have discovered that the AI/ML techniques help in fast sign-off of the power grid design problems. This chapter concludes all the proposed contributions of this thesis along with the future directions for research.

7.2 Summary of the Contributions

- **Power Grid Analysis using Probabilistic Approach:** This contribution presents a power grid analyzer based on Lévy flight principle. In this work, Lévy flight approach is used to for traversing the power grid network, which helps in obtaining a fast solution of the power grid network. We also remove the self loops in our proposed approach, which helps in fast convergence in power grid network solutions. Our proposed approach is validated using large-scale power grid benchmarks. Results show significant speedup over the Random walk and Gauss Seidel approach.

- **Design Space Exploration of Power Grid using Heuristic Approach:** In this contribution, a multi-objective framework for minimization of the IR drop-metal routing area of the VLSI PGN is proposed using evolutionary computation technique. Initially, the power grid design process and all reliability issues during the design phase are described. Subsequently, the objective function considering the IR drop and metal routing area is formulated with the consideration of reliability and yield-based design constraints. NSGA-II based multi-objective evolutionary algorithms have been employed to minimize the two objectives of the problem simultaneously and to obtain an optimum point of trade-off. Experimental results on standard IBM power grid benchmarks show that our proposed framework is able to obtain an optimum point for the IR drop and metal routing area.

- **Power Grid Design using Machine Learning:** In this contribution, we have proposed a deep learning-based framework to predict the initial power grid design. We predict the power grid interconnect width as part of the design process, which is time-consuming and tedious work. Subsequently, we also predict the worst-case IR drop in the power grid. A neural network-based multi-regression technique is used in our model for accomplishing the prediction tasks. Results on IBM power grid benchmarks show ∼6× speedup than the conventional power grid design approach.

- **Aging Prediction of Power Grid Design using Machine Learning:** This contribution presents an approach to predict the electromigration (EM)-based aging of the on-chip power grid (PG) network using a machine learning method. Neural Network regression-based machine learning technique is used to predict the mean-time-to-failure (MTTF) during the incremental design of the PG network. The training set is generated using the parameters of the PG network, and appropriate features are selected for the proposed machine learning approach by evaluating r^2 score. For generating the test dataset, a perturbation in the PG network is done. The trained model is used on the test set for MTTF prediction of different power grid benchmarks. A new failure criterion is proposed in order to improve the MTTF of the proposed model. Results on different power grid benchmark circuits show that the proposed machine learning model exhibits a significant speedup than all of the state-of-the-art EM-based MTTF prediction models.

The summary of the thesis is shown in Fig. 7.1. From the work of Chapter 5 and Chapter 6, it is also observed that machine learning approaches work well for incremental designs, where iteratively little perturbation is made in designs. In such iterative cases of design, machine learning can be utilized efficiently to predict instantly the changes that occur in the design, instead of performing all the simulations and design exploration all over again. Further, in order to fully utilize the benefit of machine learning in the design phase of on-chip power grid interconnect, more robust learning techniques need to be explored.

7.3 Limitation

The work proposed in Chapter 3 is applicable to regular large power grids. In order to adapt the proposed approach of Chapter 3 for practical cases of power grid circuits, it is necessary to have an analytical equivalent resistance model for practical non-uniform power grids.

The methods presented in Chapter 4 and Chapter 5 are designed with the assumption that it is a two-layer power grid. However, the work can be extended for a multi-layer power grid with proper formulation and calibration.

As mentioned before, the machine learning approaches are found to produce good results for incremental designs. Therefore, further work is required in order to design fully automated machine learning solutions for on-chip power grid design.

7.4 Future Works

The contributions of this thesis can be extended in several ways. Some of the possible future research directions are listed below:

- The machine learning-based proposed works in this thesis uses manual feature engineering. In future, automatic feature engineering can be employed to further automating the learning process of the power grid design.
- This thesis profoundly concentrated on formulating the problems as supervised learning problems. In the future, power grid design problems can be formulated as unsupervised learning problems and solved using the emerging learning approaches such as Variational Autoencoder, Generative Adversarial Network etc.
- Other objectives of the power grid design can further be solved using AI/ML approaches.
- Parallelization techniques can be explored for fast sign-off of the power grid analysis.
- Thermal Issues of PG Design can be explored.
- Extension of the works to PG Design of 3D IC.
- This thesis's proposed methods can also be extended to electrical grid design (used for delivering electricity from producers to consumers), with appropriate changes.

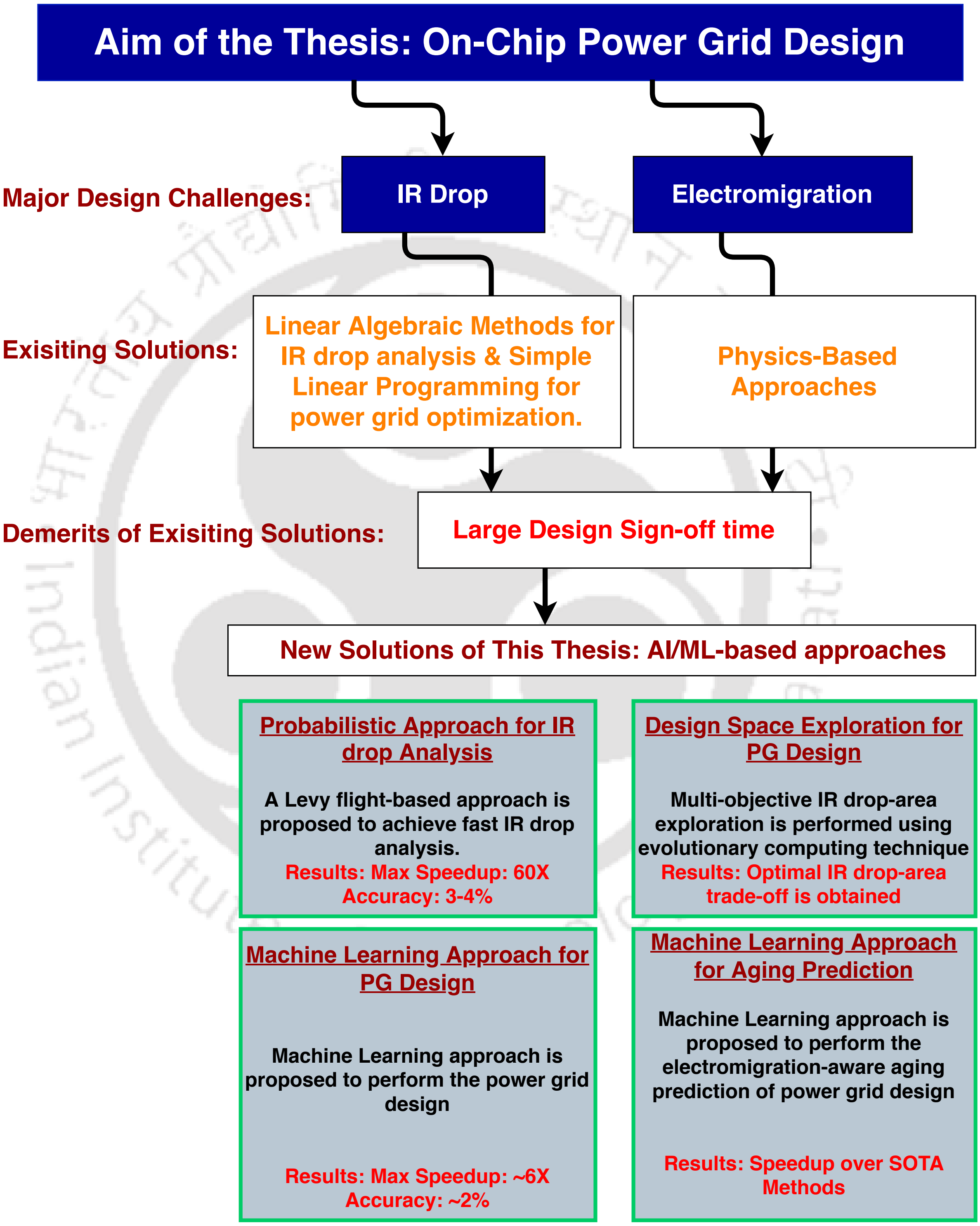

Figure 7.1: Summary of the Thesis