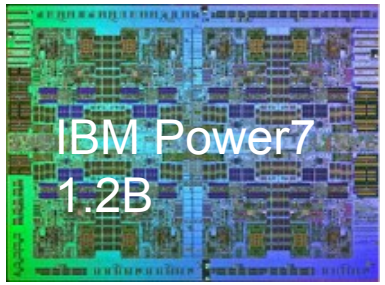
The 34th International Conference on VLSI Design &
The 20th International Conference on Embedded Systems
From The Transistor To Cyber-Physical Systems, For Solving Societal Challenges
February 20 - 24, 2021 (Virtual Event)
VLSI SOCIETY OF INDIA
#VLSID2021
www.embeddedandvlsidesignconference.org

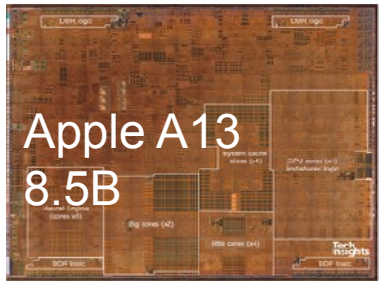
Design Methodology for On-Chip Power Grid Interconnect: AI/ML Perspective

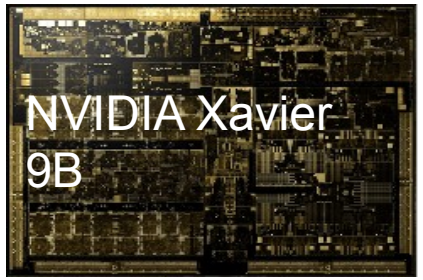
Sukanta Dey, IIT Guwahati

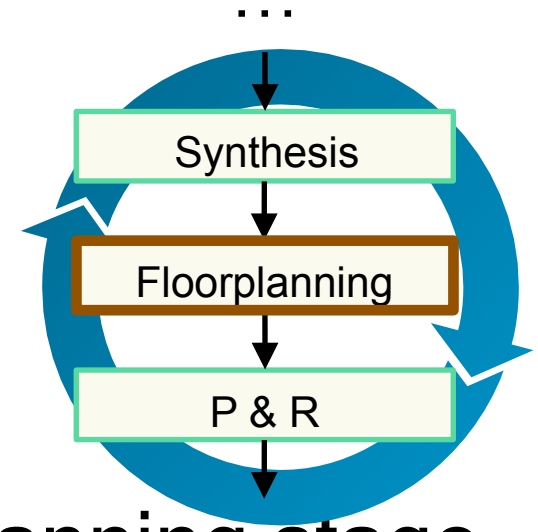
Introduction

- Modern VLSI size and complexity keeps increasing.









- Power grid interconnects are designed in floorplanning stage.
- Power Planning plays a central role in the design flow.
  - Significant impact on design closure.
  - Check and satisfy IR drop and Electromigration margin.
  - Ensure reliability of chip/power grid.

Power Grid and Electrical Models

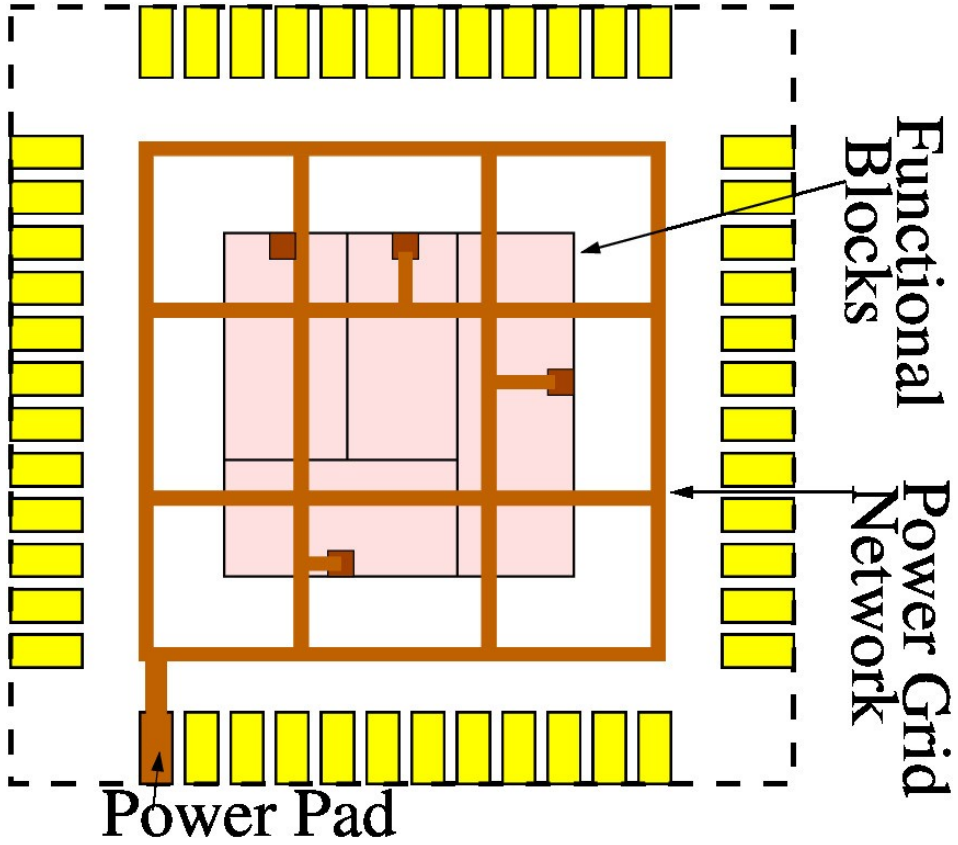


Fig: Toy model of SoC with Power Grid Connections

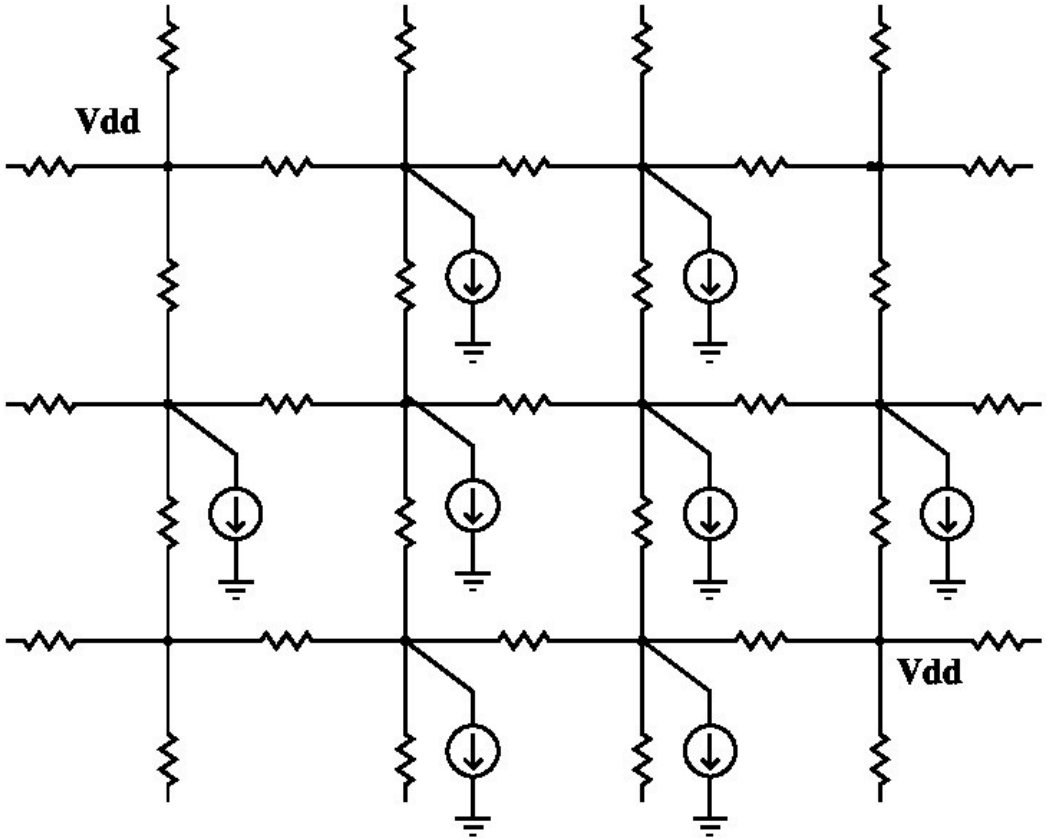


Fig: Steady-state electrical circuit model of power grids

Power Grid Design Challenges

- Large size of power grid circuit with increase in complexity.
- IR drop violations occur.
- Suffers from Electromigration violation.
- IR drop and Electromigration margin should be ensured.
- Optimal design point should be obtained.
- Existing methods are semi-automated or manual.
- Takes huge human labour and time for sign-off.
- There is a need for study in better design methodology/tool.

Contributions of my work

- **Proposed work is divided in four parts:**

1) Fast Probabilistic Power Grid Analysis Method.
2) Design Space Exploration to find optimal design point using Metaheuristics
3) ML-based Power Grid Design.
4) ML-based Aging Prediction.

Fast Power Grid Analysis*

- Power grid network is converted into a unweighted graph.
- Objective is to speed up power grid analysis process.
- Our approach is based on random walk(RW)-based technique.
- We try to remove the self-loops of random walks.
- We adapted jumping strategy to speedup the convergence.
- Levy flight is used to incorporate the jumping strategy.
- To validate the method, it is tested with 49M nodes of power grid network.
- We achieve max. speedup of 60X over RW with $\leq$4% accuracy.

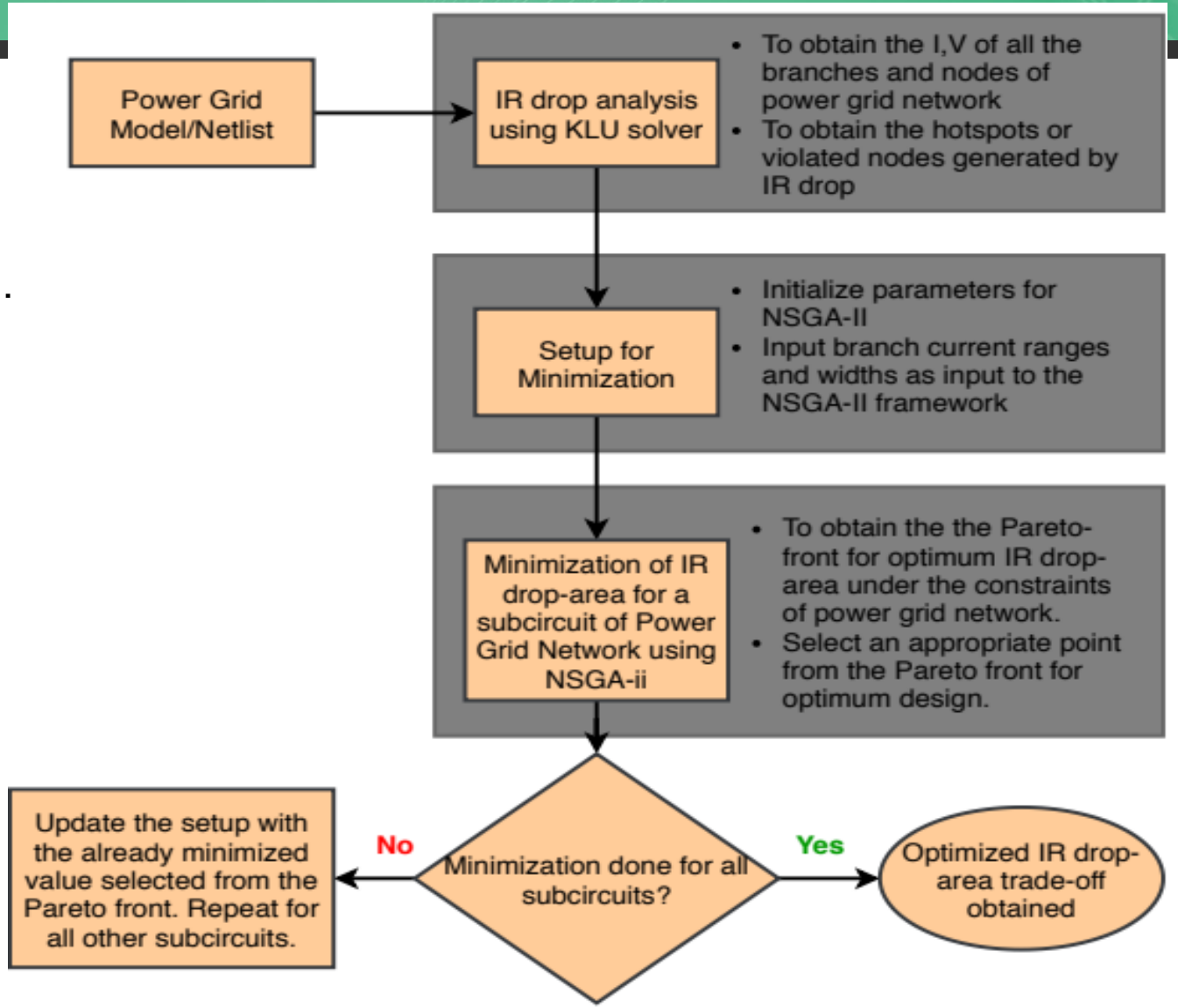
*Dey et al. **"Markov Chain Model using Levy Flight for VLSI Power Grid Analysis",** 30th International Conference on VLSI Design **(VLSID 2017),** Jan 2017.

Design Space Exploration

IR drop minimization increases metal routing area [Dey et al. **IEEE ISVLSI 2018]**

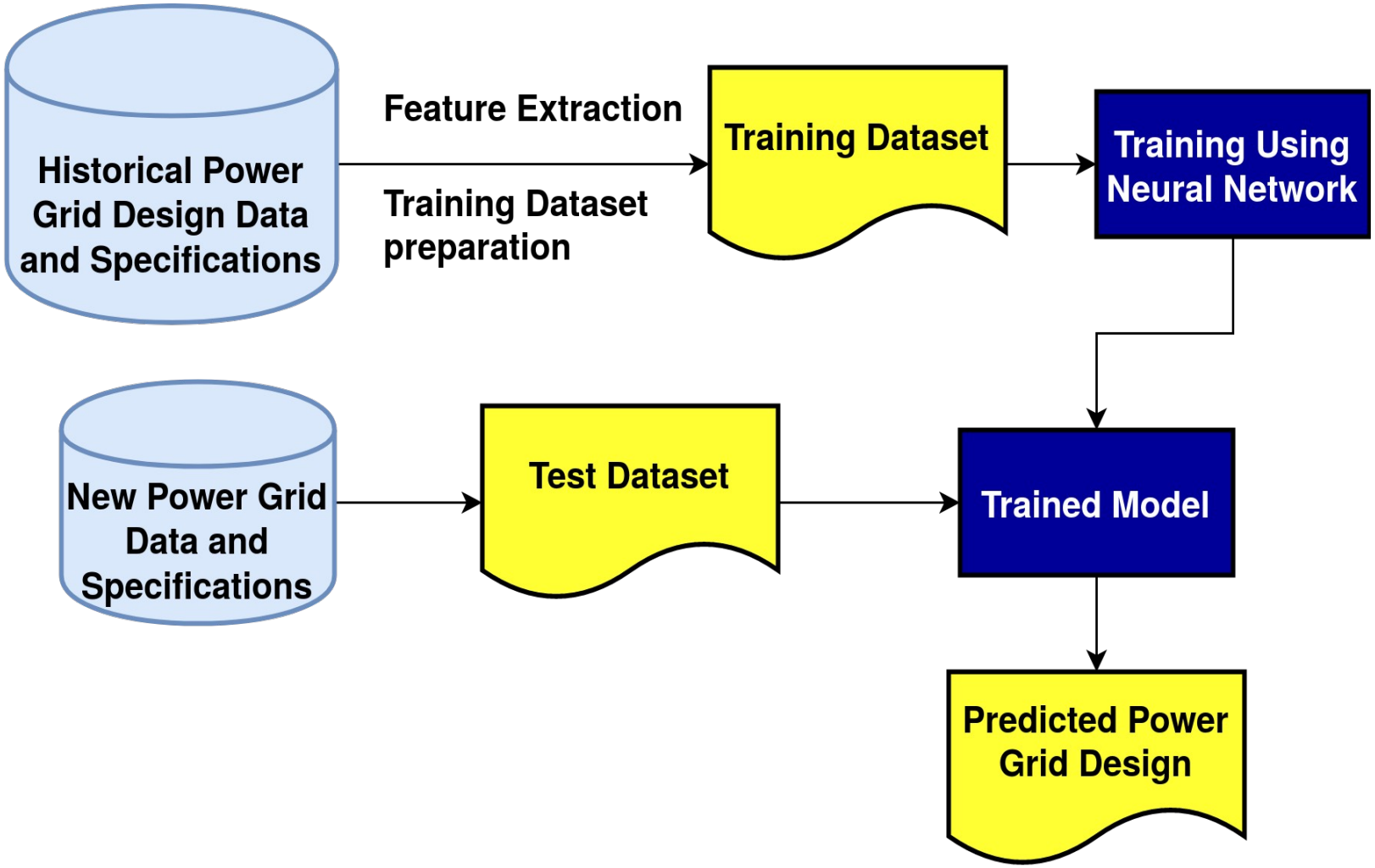
Two conflicting objectives:

IR drop and metal routing area



Optimum design point is obtained for a test case with 7.31% reduction in worst-case IR drop and 8.51% reduction in metal routing area [Dey et al. **Elsevier MICPRO 2021]**

ML-based Power Grid Design*



*Dey et al. "**PowerPlanningDL: Reliability-Aware Framework for On-Chip Power Grid Design using Deep Learning**" in **DATE'20, April 2020**.

Results

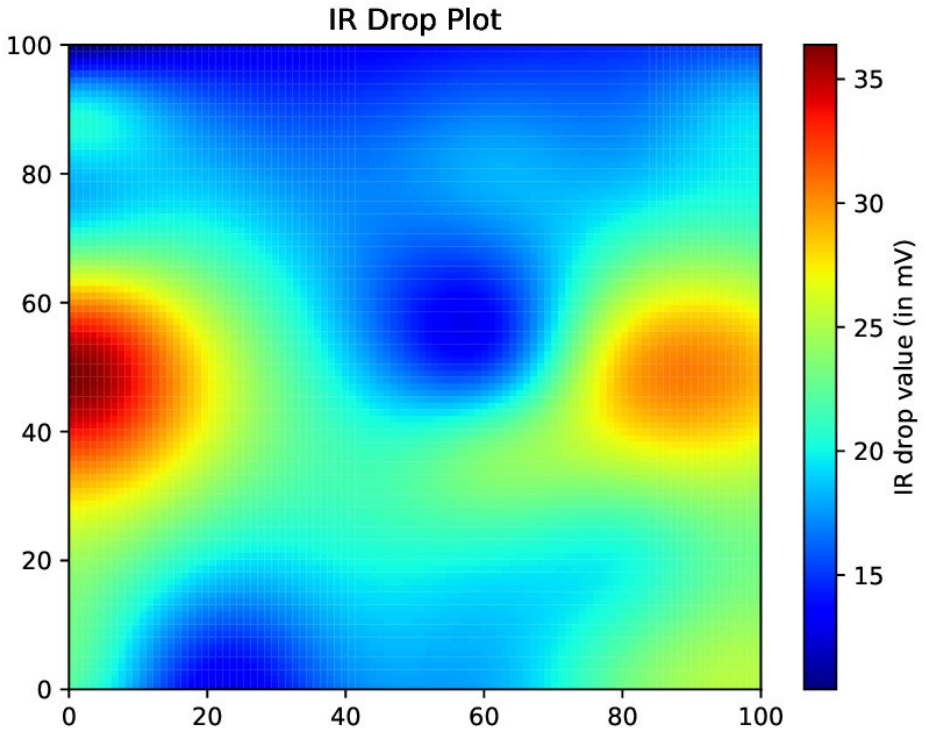


Fig: IR drop map of ibmpg2 using conventional method

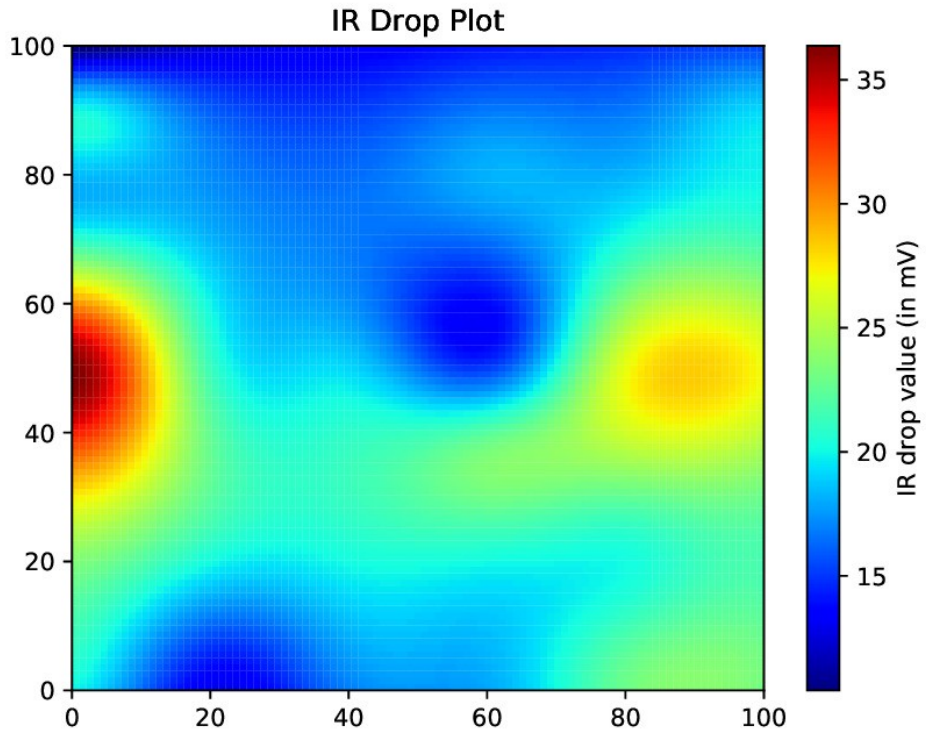


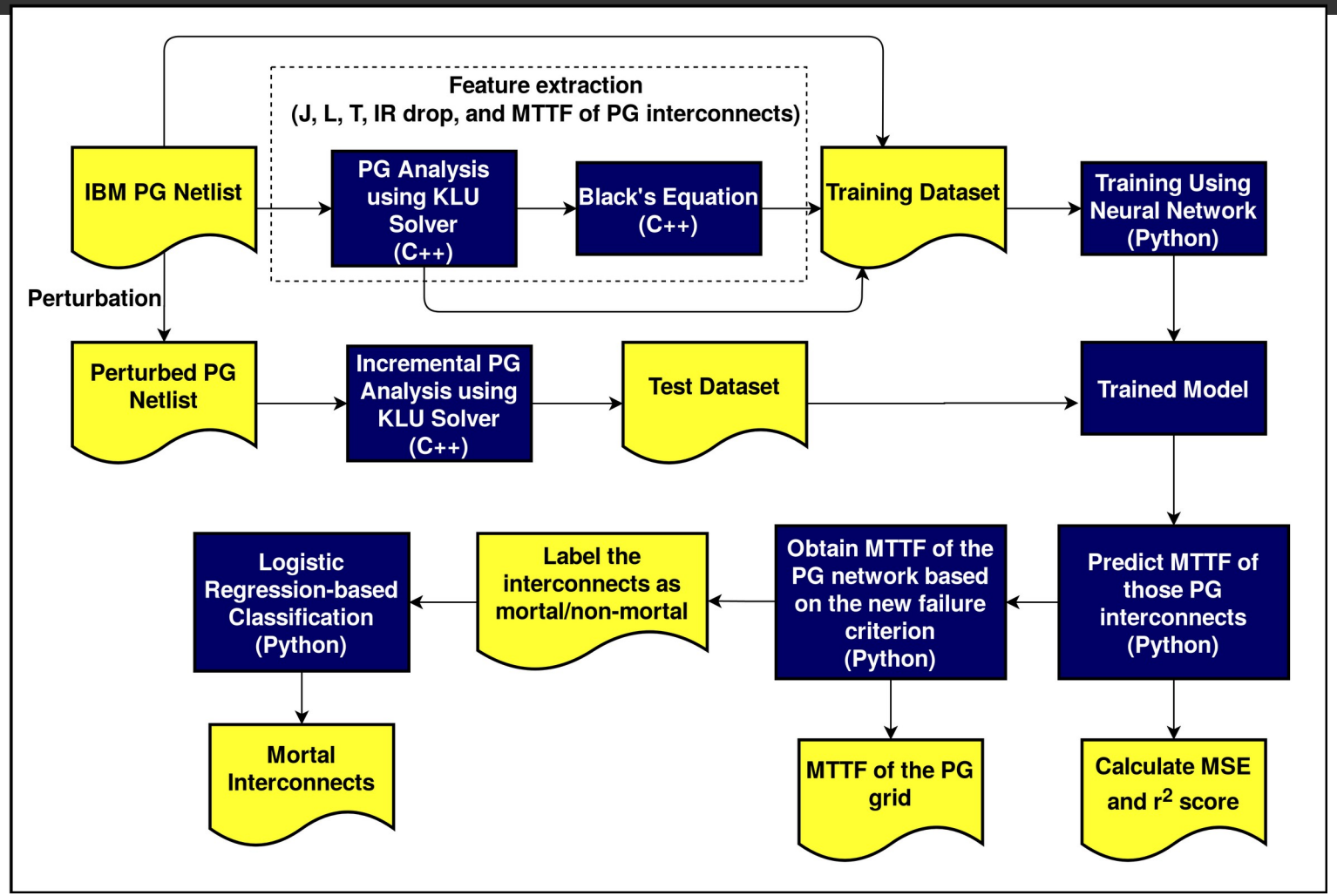
Fig: IR drop map of ibmpg2 using proposed ML approach

Same quality of results using ML!

Error ~2%

Max speedup of ~5-6X

ML-based Aging-prediction*



*Dey et al. "**Machine Learning Approach for Fast Electromigration Aware Aging Prediction in Incremental Design of Large Scale On-Chip Power Grid Network**" in **ACM TODAES, July 2020**.

ML-based Aging-prediction*

Methods	CPU Runtime (t) (Hours)					Speedup			
	TCAD2016 [19] (t_H)	ICCAD2017 [9] (t_{Ch})	TCAD2018 [10] (t_C)	IRPS2019 [30] (t_N)	Proposed (t_{ML})	$\frac{t_H}{t_{ML}}$	$\frac{t_{Ch}}{t_{ML}}$	$\frac{t_C}{t_{ML}}$	$\frac{t_N}{t_{ML}}$
PG Circuits									
PG1	0.02	0.02	0.001	0.000166	0.0001	200×	200×	10×	1.66×
ibmpg1	0.05	0.03	0.003	0.01000	0.0003	166.66×	100×	10×	33.33×
ibmpg2	0.11	0.31	0.04	0.02000	0.002	55×	155×	20×	10×
ibmpg3	5.83	4.27	0.41	0.07000	0.009	647.77×	610×	45.55×	7.77×
ibmpg4	14.71	6.81	2.31	0.11000	0.007	2,101.42×	972.85×	330×	15.71×
ibmpg5	0.69	0.25	0.06	0.03000	0.006	115×	41.66×	10×	5×
ibmpg6	1.75	2.07	0.79	0.23330	0.009	194.44×	230×	87.77×	25.92×
ibmpgnew1	16.78	0.42	1.24	0.08000	0.013	1,290.76×	32.06×	95.38×	6.15×
ibmpgnew2	15.32	2.60	0.43	0.06000	0.008	1,915×	325×	53.75×	7.50×
PG2	10.94	1.12	1.06	0.10166	0.010	1,094×	112×	106×	10.06×
PG3	-	-	-	0.13666	0.04200	-	-	-	3.25×
PG4	-	-	-	0.25666	0.10100	-	-	-	2.54×
Avg. Speedup						778×	277.85×	76.84×	10.74×

Our proposed ML-approach achieve speedup of 778X over [19], 278X over [9], 76.84X over [10], and 10X over [30].

ML-based Aging-prediction*

#VLSID2021

	MTTF (μ) (years)				
Methods	**TCAD2016 [19] (μ_H)**	**ICCAD2017 [9] (μ_{Ch})**	**TCAD2018 [10] (μ_C)**	**IRPS2019 [30] (μ_N)**	**Proposed (μ_{ML})**
PG Circuits					
PG1	14.01	6.10	8.51	6.5	13.25
ibmpg1	12.55	6.50	10.91	7.0	12.10
ibmpg2	18.75	6.78	10.11	12.1	12.55
ibmpg3	31.96	6.66	9.95	6.7	12.25
ibmpg4	33.39	9.83	11.95	16.7	17.48
ibmpg5	25.16	6.54	6.63	6.3	10.33
ibmpg6	19.87	9.53	11.96	11.2	12.41
ibmpgnew1	25.96	13.24	11.64	13.2	14.56
ibmpgnew2	21.80	5.72	6.72	7.3	13.24
PG2	17.85	8.32	9.32	10.3	11.21
PG3	-	-	-	7.2	10.51
PG4	-	-	-	6.8	8.47

Accuracy wise our ML approach is the closest to accurate method of TCAD2016, and better than all other SOTA results.

Publications

#VLSID2021

- **Sukanta Dey**, Sukumar Nandi, Gaurav Trivedi, "**PGOpt: Multi-objective Design Space Exploration Framework for Large-Scale On-Chip Power Grid Design in VLSI SoC using Evolutionary Computing Technique**" in **Microprocessors and Microsystems (MICPRO), Elsevier**, Vol. 81, Article 103440, March 2021.
- **Sukanta Dey**, Sukumar Nandi, Gaurav Trivedi, "**Machine Learning Approach for Fast Electromigration Aware Aging Prediction in Incremental Design of Large Scale On-Chip Power Grid Network**", **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Vol. 25, No. 5, Article 42, July 2020.
- **Sukanta Dey**, Sukumar Nandi, Gaurav Trivedi, "**PowerPlanningDL: Reliability-Aware Framework for On-Chip Power Grid Design using Deep Learning**", **IEEE/ACM Design, Automation and Test in Europe (DATE 2020),** Grenoble, France, 9-13th March 2020, pp. 1520-1525.
- **Sukanta Dey**, Satyabrata Dash, Sukumar Nandi, Gaurav Trivedi, "**PGIREM: Reliability-Constrained IR Drop Minimization and Electromigration Assessment of VLSI Power Grid Networks using Cooperative Coevolution**", **17th IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2018)**, Hong Kong SAR, China, 9-11th July 2018, pp. 40-45, IEEE.
- **Sukanta Dey**, Satyabrata Dash, Sukumar Nandi, Gaurav Trivedi, "**Markov Chain Model using Levy Flight for VLSI Power Grid Analysis**", **30th International Conference on VLSI Design (VLSID 2017)**, Hyderabad, India, 7-11th January 2017, pp. 107-112, IEEE.
- **Sukanta Dey**, Sukumar Nandi, Gaurav Trivedi, "**PGRDP: Reliability, Delay, and Power-Aware Area Minimization of Large-Scale VLSI Power Grid Network using Cooperative Coevolution**", in the **Book: Intelligent Computing Paradigam - Recent Trends, Springer** (Chapter 6), 2019.

THANK YOU

THE 34TH INTERNATIONAL CONFERENCE ON VLSI DESIGN
&
THE 20TH INTERNATIONAL CONFERENCE ON EMBEDDED SYSTEMS
(VLSID 2021)

https://embeddedandvlsidesignconference.org